Transformational Silicon Electronics

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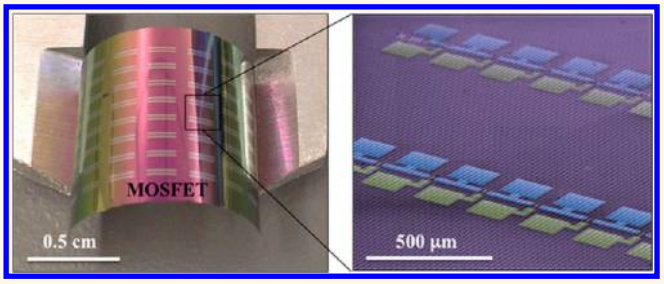
Integrated Nanotechnology Lab, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia. M.H. conceptualized and directed the project. J.P.R. fabricated the MOSCAPs, MIMCAPs, and MOSFETs and carried out the experiments. G.A.T.S. developed the wafer recycling process and fabricated the thermoelectric generators. S.B.I. and A.M.H. characterized the thermoelectric generators. S.M.A. fabricated the microlithium ion battery. All analyzed and discussed the data. J.P.R. and M.M.H. coauthored and all provided inputs on the paper.

ABSTRACT In today's traditional electronics such as in computers or in mobile phones, billions of high-performance, ultra-low-power devices are neatly integrated in extremely compact areas on rigid and brittle but low-cost bulk monocrystalline silicon (100) wafers. Ninety percent of global electronics are made up of silicon. Therefore, we have developed a generic low-cost regenerative batch fabrication process to transform such wafers full of devices into thin (5 μm), mechanically flexible, optically semitransparent silicon fabric with devices, then recycling the remaining wafer to generate multiple silicon fabric with chips and devices, ensuring low-cost and optimal utilization of the whole substrate. We show monocrystalline, amorphous, and polycrystalline silicon and silicon dioxide fabric, all from low-cost bulk silicon (100) wafers with the semiconductor industry's most advanced high-κ/metal gate stack based high-performance, ultra-low-power capacitors, field effect transistors, energy harvesters, and storage to emphasize the effectiveness and versatility of this process to transform traditional electronics into flexible and semitransparent ones for multipurpose applications.



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Flexible electronics is an emerging field with great potential for a variety of applications ranging from *in vivo* biomedical applications to wearable smart bionics. Naturally, polymer-based plastic has been used as a substrate for such activity.[1,2] Low cost and simplified process technology made organic devices on plastic-based substrates popular. Nonetheless, due to limited thermal budget and stability during processing and operation, respectively, and the inherent low electron mobility of plastic, its expansion beyond display and sensor technologies is yet to be demonstrated. A different alternative has been explored recently, where competitive mobilities can be achieved through carbon-based 2-D and 1-D materials such carbon nanotubes (CNTs) and graphene.[3,4] Fully printed transistors with semiconductor-enriched single-walled carbon nanotubes (SWNTs) have been fabricated with mobility nearing 10 $cm^2/(V\ s)$.[5] Although their potential to be adapted into a roll-to-roll configuration for low-cost implementation seems encouraging for macroelectronics, their performance, operation voltage, and integration level are still very far from being compared with state-of-the-art, nanoscale, ultradense, silicon-based transistors, which are the foundation of high-performance electronics in portable devices. Since 2004, John Rogers' group has demonstrated transfer technique based monocrystalline silicon nanoribbons, building exciting devices and systems such as hemispherical eyes and implantable cardiograms.[6−8] Especially, they have successfully transferred the new knowledge into technology for mainstream photovoltaic applications and others.[9] These techniques use expensive [compared to bulk silicon (100)] silicon on insulator (SOI)[10,11] or unorthodox silicon (111).[9] One unique area of improvement for the transfer technique is to be able to comply with the ultra-large-scale-integration (ULSI) density required for modern electronics. Therefore, scientific exploration and technology expansion opportunities exist for integrating the silicon industry's two most profound applications, electronics and microelectromechanical systems (MEMS), onto a flexible platform.

In the recent past, three groups have capitalized on full silicon wafer peel-off with

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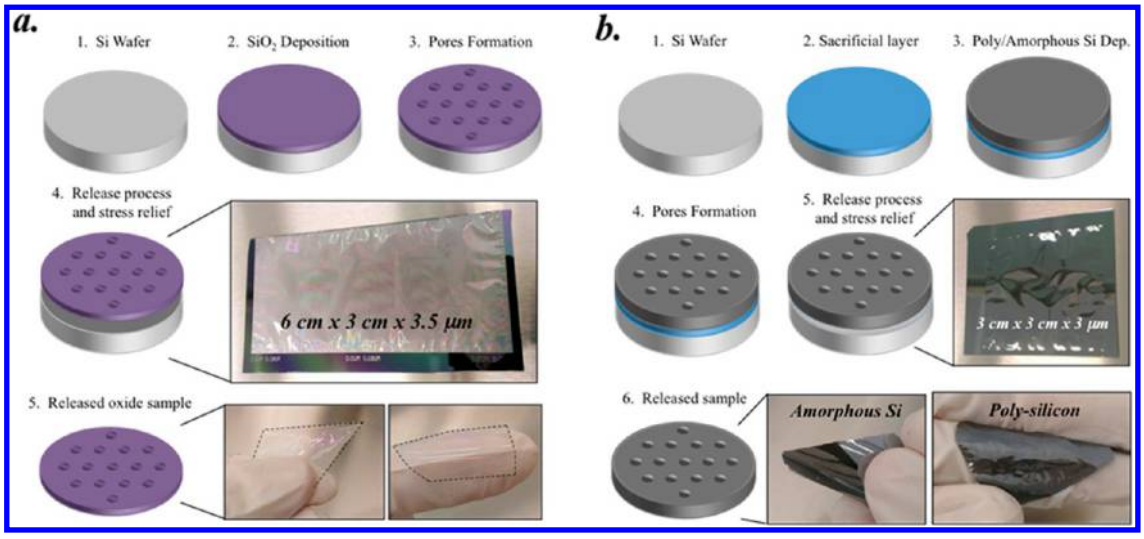

Figure 1. Fabrication process flow of silicon dioxide fabric, including digital photographs of a 18 cm^2 silicon dioxide membrane before (step 4) and after (step 5) release from the carrier wafer (a). Fabrication process flow of polycrystalline/amorphous silicon fabric, including digital photographs of 9 cm^2 amorphous and polysilicon fabrics before (step 5) and after (step 6) release from the carrier wafer (b).

prefabricated devices. The first one generates porous silicon and then grows epitaxial silicon to fabricate devices before peeling off small areas from the full wafers;[12] the remaining two depend on dopant introduction into the bulk wafers before fabrication of devices or deposition of a "releaser" thin film deposited on top of already fabricated devices and then peel-off by the mechanical force of stress mismatching.[13−16] Definitely all these techniques are advancements in the area of flexible electronics. Still, from a cost consideration perspective epitaxy and dopant introduction (like the Smart Cut or SIMOX process) are processes yet to be cost-effective. Moreover, there is a potential device damage probability related to the peel-off process, like with other demonstrations such as back grinding. Finally the process shows limited bendability and opaqueness. In all these cases, the remaining wafer after release from the substrate is not used further, leading to higher cost with respect to plastic-based "garage fabrication"-oriented flexible electronics.

On the other hand, one seemingly easy solution is to use commercially available ultrathin flexible silicon wafers. However, (i) they require special care during their handling, (ii) they can deform in an enhanced fashion when subjected to high thermal budget, (iii) they have more defects compared to standard bulk silicon wafers used for electronics applications, and (iv) they are expensive. Therefore, we report a generic simple batch fabrication process to release flexible and semitransparent silicon fabric with pre- or post-release devices from bulk monocrystalline silicon (100), amorphous and polycrystalline silicon, and silicon dioxide. We used thermal oxidation, thin film deposition such as plasma-enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD) and reactive ion etching as baseline microfabrication techniques. Our process allows us to recycle the remaining wafer by chemical mechanical polishing for further processing, making it economically more attractive. We also demonstrate high-k/metal gate stack based metal oxide semiconductor capacitors (MOSCAPs), field effect transistors (MOSFETs), metal−insulator−metal capacitors (MIMCAPs), microfabricated lithium ion batteries, and thermoelectric generators on silicon fabric.

RESULTS

Our generic process can be pursued in two ways depending upon the selectivity of the material to be released with respect to a silicon (100) carrier wafer. First, materials such as silicon dioxide (SiO_2), which are selective to silicon, can be directly deposited on top of the carrier wafer. In our case we first deposited 3.5 μm of SiO_2 using PECVD (Figure 1a2). Next, we etched pores through photolithography and reactive ion etching (RIE), which serve as etch holes (Figure 1a3), so the silicon below the oxide is removed, releasing the top membrane. As stated, XeF_2 is used to selectively etch the silicon without affecting the oxide (Figure 1a4). Other materials such silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), and the like can use this approach to form released membrane-like thin films. This shows the unique versatility of the process for formation of flexible dielectrics of both low- and high-k permittivity.

The second approach refers to materials that cannot be selectively etched with respect to silicon. Such is the case of polycrystalline silicon and amorphous silicon. In these cases, an additional layer is introduced, a sacrificial layer, which will be removed in order to release the upper layer. In a sense we are generating a virtual silicon-on-insulator wafer, where the buried oxide represents the sacrificial layer. Thus, the process consists in

the deposition of 200 nm of SiO_2 (Figure 1b2) followed by 3 μm of polycrystalline or amorphous silicon (Figure 1b3). Both depositions are done through a PECVD system. Next, we etched pores or etch-holes through the top layer (Figure 1b4), and then an isotropic etchant is used to remove the buried oxide layer, releasing the membrane on top (Figure 1b5).

We would like to point out that all the pores, or etch-holes, are defined lithographically to achieve specific densities and micrometric dimensions in a controllable and regular fashion with mass production capabilities. Thickness can be easily defined by controlling the amount of material deposited or the depth of the channels etched into the substrate in the case of monocrystalline silicon.

We have reproducibly fabricated amorphous silicon, polycrystalline and monocrystalline silicon, and silicon dioxide fabrics with a pore size of 5 μm regularly separated by 5 μm spacing between them, 5−20 μm in thickness and from 9 to 18 cm^2 in size. Figure 1a shows a piece of SiO_2 before and after peel-off from the carrier wafer. As can be appreciated form the figure, the film exhibits semitransparency and flexibility. On the other hand, Figure 1b shows both amorphous and polycrystalline silicon membranes with dimensions of 3 cm by 3 cm and 3 μm in thickness. An important point to clarify is that stress can be built up during the deposition of the films, and so it can cause the films to roll up after release. To overcome this issue, an annealing step at a temperature that depends on the specific material is required. For example, in the case of SiO_2, it has been found that an annealing at 950 °C for 30 s can help to release most of the stress.[17]

In a second stage, we have expanded our technique to release a thin film of monocrystalline silicon. We have developed an alternative method where we use only a low-cost but most widely used silicon (100) wafer and introduce the formation of spacer-based pore protection, so we are able to avoid the use of a much more expensive SOI wafer. This process has been described in detail in a prior work.[18]

In summary we fabricate first the desired devices, followed by a hard mask deposition, trench etching through the hard mask and the silicon by deep reactive ion etch (DRIE), formation of a vertical sidewall (spacer) from an insulating (dielectric) material to protect the trench's sidewall, followed by XeF_2-based isotropic etch into the silicon substrate to release the upper detached silicon piece with devices. The piece is now mechanically flexible due to its reduced thickness and optically transparent due to the trench formed during the DRIE process. Furthermore, the remaining wafer can be recycled to fabricate more devices for a better cost-effectiveness of the material (Figure 2).[19]

We have developed furnace-based SiO_2 and ALD-based Al_2O_3-formed spacers. Furnace oxide is robust but suitable only with materials that can withstand high thermal budget processing. We typically use furnace oxide for a release-first/device-second kind of approach: a fast device implementation scheme where we first release the sample while there are no thermally restrictive materials and then deposit and pattern thin film stacks to build the devices. The challenge with this approach is the nonuniformity of the photoresist coating due to the wavy nature of the released sample, which can translate into nonuniformity during the etching process. Normally a thicker photoresist helps to improve this issue. We have used this approach to fabricate MOSCAPs and MIMCAPs.[20−23]

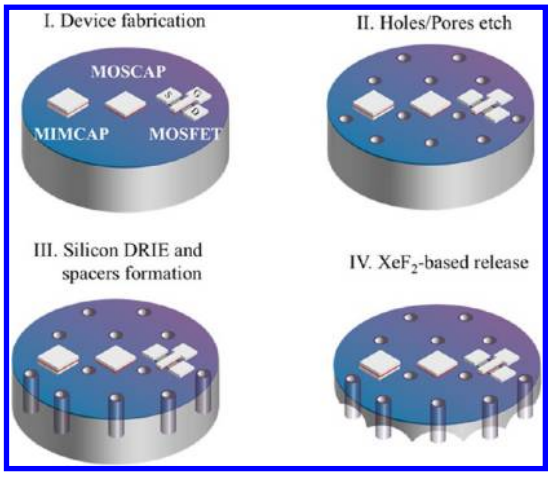

Figure 2. Generic flow to transform conventional silicon electronics into flexible and semitransparent ones.

For low temperature process compatible devices we use ALD-based Al_2O_3 spacers where the thermal budget is relatively smaller than that of furnace oxidation. Our ALD Al_2O_3 process can be carried out at temperatures between 150 and 250 °C. Thus, we use this process with a device-first/release-last scheme, where we have the advantage of a precise alignment between holes and devices. MOSCAPs and MOSFETs have been demonstrated though this scheme.[18] PECVD-based oxide was also evaluated since it performs at relatively low temperatures (250 °C); however, due to its not very conformal nature and defect density, it was not a suitable option for spacer formation.

DISCUSSION

Since performance per cost has driven Moore's law based traditional silicon electronics, the same metric will also drive the growth of flexible electronics. Therefore, we have paid extra attention to ensure reuse of the remaining silicon wafer when the top layer is released (detached) from the bottom substrate. After releasing the whole 4-inch silicon wafer (see the Supporting Information: a movie showing full 4-inch wafer release using our process), we used chemical mechanical polishing (CMP) to polish the remaining wafer to fabricate the next set of devices on that polished substrate. After the release of this new set

of devices, we apply the same CMP process to polish the remaining wafer and continue recycling it. It is to be noted that special care is required to fabricate devices as well as CMP for the last two fabrics of a traditional silicon wafer, which is typically 0.5 mm thick. Laterally from each fabric we have an area loss of 16% due to trenching (note that the trenches are made in unused areas of a chip). However, with five to six fabric formations from each 0.5 mm thick wafer, we effectively achieve five extra wafers, lowering the cost dramatically. The rise of silicon electronics is driven by the integration density (directly benefitting enhancing multitasking capability of integrated circuits), which essentially translates to bit (information/data unit)/cost, and because of this ULSI density, plastic or any other electronics cannot compete in the context of bit/cost.

Figure 3a shows a high-k/metal gate stack based MOSCAP and MIMCAP, fabricated with the release-first/device-last approach. We first release a silicon (100) fabric of 18 cm^2 in area and 20 μm in thickness, followed by cleaning and preparation of the substrate for subsequent steps. It is necessary to clarify that the fabric, although released, is still attached to the carrier wafer as in Figure 1b5, so an easy handling is still possible. Next, the stack materials that will confirm the devices (Al_2O_3/TaN in the case of MOSCAP or TaN/Al_2O_3/TaN for MIMCAP) are deposited with an ALD system. A layer of Al is subsequently deposited to serve as contact. Finally, photolithography and RIE are used to pattern the materials' stack and create the devices. The released silicon (100) fabric can be then separated from the carrier wafer by controllably breaking its edges.

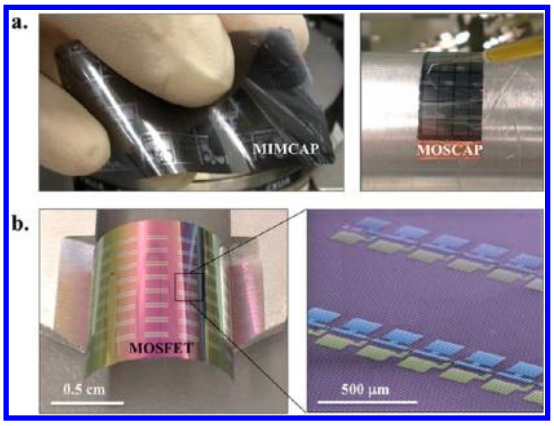

Figure 3. Digital photographs of already released, flexible MIMCAP and MOSCAP (a) and MOSFET including SEM image zoom-in of the devices (b).

Additionally, a MOSFET fabricated with the device-first/release-last approach is shown in Figure 3b. In this case we first created the active areas and then deposited and patterned aluminum oxide (Al_2O_3), as a high-k dielectric, and tantalum nitride (TaN), as metal gate, using ALD, photolithography, and RIE. We have also formed industry standard spacers along the sidewall of the gates. Next, an ion implantation process formed the source and drain areas. For contact engineering we have used nickel silicide. All the devices are contacted using aluminum. The source−drain activation anneal was completed at 950 °C for 30 s, and the device fabrication was completed with forming gas anneal (FGA) at 450 °C for 30 s, showing the compatibility of the process with high thermal budget processes needed to achieve high performance. The final step is then to release the already fabricated transistors by first etching holes in the spaces between devices, then forming ALD-based spacers for the wall's protection and finally releasing by XeF_2 etching.

Some benchmark characteristics of the released fabricated devices are shown in Figure 4a−c. MOSCAPs are an indispensable vehicle to characterize the performance and optimize the dielectric and metal gate to be used on transistors. From Figure 4a we back-calculated the dielectric thickness from the capacitance at accumulation, getting an effective oxide thickness (EOT) as small as 3 nm. A reported standard deviation of 1 nm[20] of several devices over the 18 cm^2 released sample indicated certain nonuniformity in the dielectric layer, which can be improved through optimization of the deposition technique and by replacing the metal gate deposition from sputtering with a gentler and

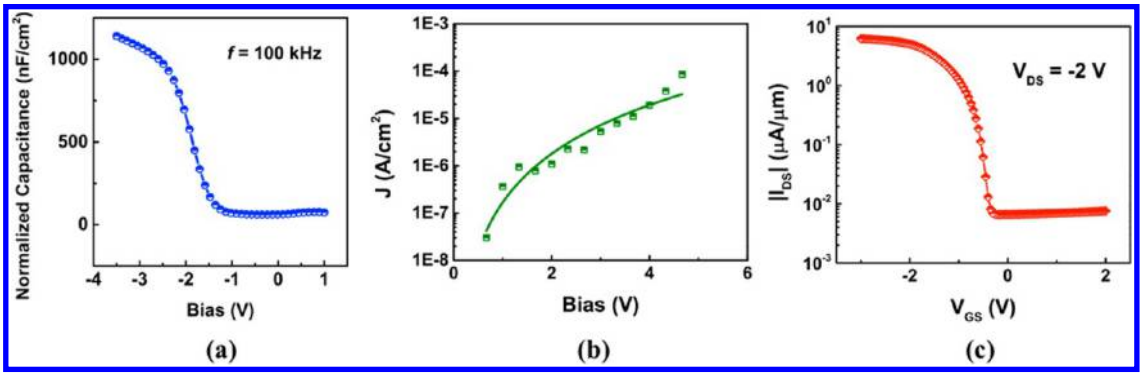

Figure 4. Benchmark characteristics of MOSCAP *C*−*V* (a), MIMCAP *J*−*V* (b), and MOSFET I_d−V_g (c) from fabricated devices. The measurements were taken after release.

higher quality ALD system. Additionally, flatband voltage was obtained using the Mott−Schottky relation and was found to be −1.57 V. MIMCAPs are very important blocks in dynamic random access memory (DRAM) due to the fact that higher capacitances per unit area can be achieved without compromising current leakage. We achieved a very small current leakage density of 1×10^{-6} A/cm^2 at 2 V with the proposed set material stack (Figure 4B). Finally, transfer (I_d−V_g) characteristics of a p-MOS field effect transistor—building blocks of today's technology—are shown in Figure 4C. The achieved current at saturation for this particular device was −6.2 μA/μm with an on/off ratio of 3 decades, threshold voltage of −0.36 V, and subthreshold swing of 145 mV/dec. This shows competitive metrics with the available set of materials and tools, and further improvement can be achieved through optimization and more advanced infrastructure. Further and more detailed analysis on released/unreleased devices, including data with different bending radii, can be found in previously published articles.[20−23]

Figure 5a,c shows a microfabricated thermoelectric generator with bismuth telluride and antimony telluride p- and n-metal thermopiles. The fabrication was based on a device-first/release-last approach on an oxidized silicon (100) wafer. First, thermopiles are formed by a two-step photolithography, sputtering, and lift-off technique of first n-type thermopiles followed by p-type thermopiles. Next, a protection layer is deposited to protect the thermopiles, leaving opening areas for the metallic connector pads. Finally, holes are created for the release process, holes' wall-protection is done with ALD-based spacers, and then the release is performed with an isotropic etchant.

Furthermore, a lithium ion battery was fabricated with a release-first/device-last approach. A 25-μm-thick silicon fabric is released with the method previously mentioned, followed by the deposition of a platinum (Pt) current collector and $LiCoO_2$ cathode. Then a LiPON-based anode is deposited and immediately after a Ni electrode. Finally, parylene is deposited to protect the moisture-sensitive materials (Figure 5d,e). Again, high flexibility was observed (measured bending radius was 0.75 cm) (Figure 5b). After release, up to 7 times higher voltage is generated with a 20 °C difference, and a charging capacity of 1.2 μAh at a maximum voltage of 0.3 V was achieved (Figure 5c,e). It is to be noted that we are still optimizing our processes for both of these devices, and only the preliminary characteristics are shown. Nonetheless the process integrity and effectiveness are demonstrated for fabricating such devices on a flexible silicon fabric with our two different approaches.

Regarding the release process, due to its properties, qualities, and cost, XeF_2-based etching acts as an ideal method for the release of our sensitive samples. First of all, due to its chemical nature, it does not require ion bombardment or an external energy source, and it exhibits a high selectivity to diverse dielectrics, metals, and polymers used in traditional integrated circuit processing, making it easy to integrate for post-CMOS micromachining. Furthermore it does not require high temperature, and it is possible to achieve very fast etch rates.[24]

On the other hand, XeF_2-based etching turns out to be an interesting solution pricewise. In order to release

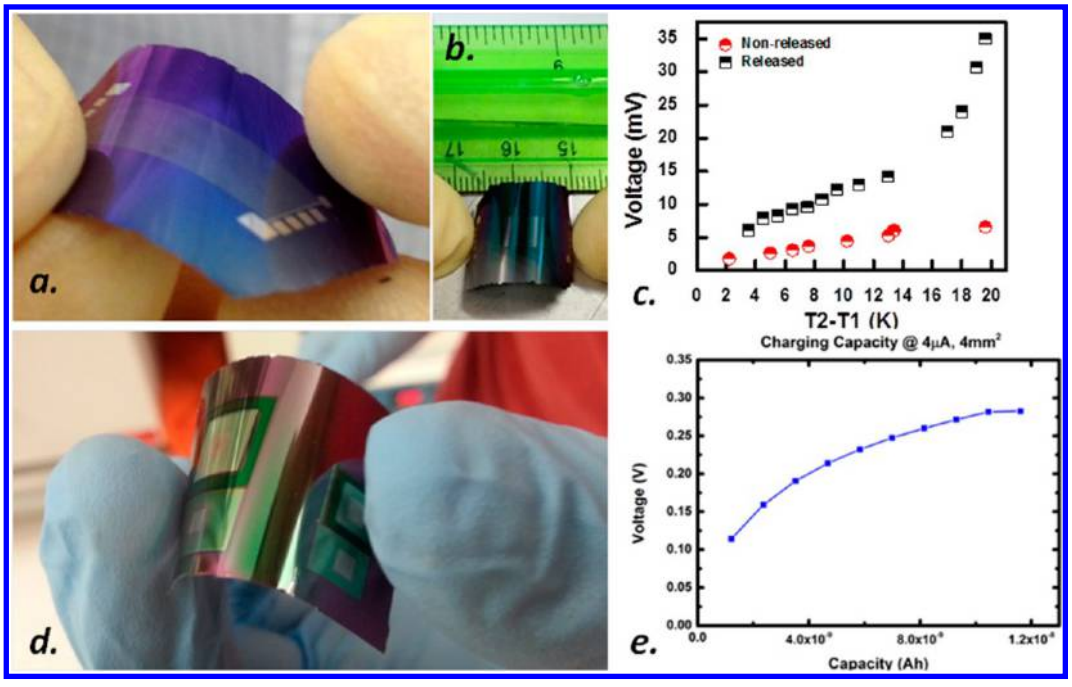

Figure 5. Microfabricated thermoelectric generator (a, b) and lithium ion battery (d) are fabricated on flexible silicon and silicon oxide fabric, respectively. Initial device characteristics (c, e) show promising yield.

a 6 cm by 3 cm silicon fabric, only about 2 g of XeF_2 is consumed (100 cycles, 30 s/cycle). If we consider that the cost of XeF_2 is about $8 per gram (Pelchem SOC Ltd.), which is comparable to the cost of xenon gas itself, then we are only adding $0.88 per cm^2 released to the final cost. In fact, if xenon gas is reclaimed from the exhaust, most of the cost of the XeF_2 used during etching could be recovered.[25]

Alternatively, wet etchant options are available, and although they might look attractive from a cost perspective, handling and postcleaning would be a pressing concern during the release process due to the sensitivity of the samples. Moreover an appropriate wall protection would need to be developed and optimized according to the etchant's selectivity.

CONCLUSION

Flexible and transparent electronics is an emerging field for multipurpose applications. Bright resolution displays, sensors, and energy and biomedical electronics have been successfully demonstrated predominantly on plastic or similar materials. Researchers have used organic molecules, transfer of nanomembranes, self-assembly, back grinding, porous silicon formation followed by epitaxial film growth, spalling by using a stressor, and using buffer sacrificial layers to demonstrate such applications. A multitude of substrates of various materials such as silicon-on-insulator, silicon (111), and III−V materials have been used. At the same time, the growth of today's electronics-oriented world has been based on bulk silicon and its various formats: monocrystalline (100), amorphous, and polycrystalline. It is therefore important to develop a generic process to transform rigid and brittle silicon-based electronics into flexible and transparent ones. Therefore, we have shown a generic low-cost batch fabrication process based on standard microfabrication techniques to fabricate thin (>5 μm), mechanically flexible, optically semitransparent silicon fabric with pre- or postreleased devices without any thermal budget limitation. We have used the technique to demonstrate monocrystalline silicon (100), amorphous and polycrystalline silicon, and silicon dioxide fabric. We have also shown a set of representative devices—the semiconductor industry's most advanced high-k/metal gate stack based metal oxide/insulator semiconductor/metal capacitors (MOSCAPs and MIMCAPs), field effect transistors, and thermoelectric generators—to emphasize the effectiveness and versatility of this process for nearly all silicon-based electronics that can be fabricated on regular bulk silicon wafers, which eventually can be transformed into a flexible and semitransparent electronics. Enabling the world's growing population to better access information sources (such as cloud computation) needs a rapid expansion of affordable high-performance, ultra-low-power, multifunctional, widely deployable (flexible format would be a game changer) electronics, and thereby our demonstration can contribute significantly to transform the state-of-the-art silicon electronics into flexible and semitransparent ones. Furthermore, due to the CMOS compatibility of our procedure, it allows the unique opportunity of using ULSI techniques with nanoscale architecture and state-of-the-art materials, thus enabling the development of a truly high-performance, flexible computation. We have demonstrated the compatibility of the detailed processes for microsize devices, and thus the process can be easily deployable for nanoscale devices.

METHODS

In the case of silicon dioxide (SiO_2) membranes we started by depositing 3.5 μm of SiO_2 using PECVD: 66 nm/min, 300 °C, 20 W_{RF}, 1000 mTorr, 6 sccm SiH_4, 850 sccm N_2O, 163 sccm N_2. Next, we used photolithography and RIE to create etch holes: 15 min, 1500 W_{ICP}, 100 W_{RF}, 10 mTorr, 40 sccm C_4F_8, 5 sccm O_2. Finally, the release process is done with XeF_2-based etch: 4.5 Torr, 50−100 cycles, 30 s/cycle.

Poly/amorphous Si membranes are fabricated starting with the deposition of 200 nm of SiO_2 by PECVD (66 nm/min, 300 °C, 20 W_{RF}, 1000 mTorr, 6 sccm SiH_4, 850 sccm N_2O, 163 sccm N_2) followed by 3 μm of PECVD poly-Si (37 nm/min, 650 °C, 10 W_{RF}, 1000 mTorr, 50 sccm SiH_4, 450 sccm Ar) or amorphous-Si (42 nm/min, 250 °C, 20 W_{RF}, 800 mTorr, 30 sccm SiH_4, 475 sccm Ar). Next, etch-holes are formed by photolithography and RIE: 1500 W_{ICP}, 100 W_{RF}, 10 mTorr, 15 sccm SF_6, 5 sccm O_2. Finally, the release is done with an isotropic etchant: vapor hydrofluoric acid at 40 °C for 10 min.

Details on the fabrication and characterization of MOSCAPs, MIMCAPs, and MOSFETs can be found in our previous works.[20−23]

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Movie file showing full 4-inch wafer release using our process. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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